In the Drawings

Please replace Figures 4 and 5A-5D with the corrected drawings sheets attached hereto.

Remarks

Claims 1-3 are pending in the subject application. By this Amendment, claim 3 has been amended. New drawings are presented and the specification is amended above to reflect that. The undersigned avers that no new matter is introduced by this amendment. Upon entry of these amendments, claims 1-3 will be before the Examiner. Favorable consideration of the pending claims is respectfully requested.

The drawings are objected to at pages 2-3 of the latest Office Action. Submitted herewith are corrected drawing sheets in compliance with 37 CFR 1.121(d). Figures 4, 5A-5D have been amended to show a "semiconductor substrate". The specification has been correspondingly amended to include a reference number for the "semiconductor substrate". Applicant asserts no new matter has been added by these amendments.

The objection to Claim 3 has been obviated by the above amendment, which was in accord with the Examiner's suggestion. Applicant thanks the Examiner for his careful reading of the subject application, and for suggesting the curative amendment.

Claims 1 and 3 are rejected under 35 USC §102(e) as being anticipated by Lehmann *et al.* (U.S. 2004/0217441). Applicant respectfully transverses because Lehmann *et al.* does not teach each and every limitation of the subject invention as claimed in claims 1 and 3.

The Office Action, at page 4, states that "Lehmann *et al.* teach (Figure 4) a semiconductor device ([0054]) comprising: a capacitor having a bottom electrode **225** ([0076]), a dielectric layer **224** (anti-fuse layer is a dielectric: see [0080]) and an upper electrode **221**([0080]) formed on a semiconductor substrate **201** ([0078]); . . . ." This is incorrect. A careful reading of Lehmann *et al.* shows that the reference does not teach a capacitor as named in claim 1 of the subject application. Rather, Lehmann *et al.*, at paragraph [0079], discloses that "[s]emiconductor device **200** contains an arrangement of at least two antifuses (as shown) of the same type in vertically stacked, e.g., generally vertically aligned, relation, such as a lower contact (dual damscene) antifuse **221** and an upper contact (dual damascene) antifuse **222**, which share a common intermediate electrode **223** therebetween, . . ." (underline added for emphasis). Regarding the lower contact dual damscene antifuse, Lehmann *et al.*, at paragraph [0080], explains that "[l]ower contact antifuse **221** has a lower fusible insulator portion . . . formed on top surface **202** of wafer **201** and defining a thin lower contact fuse element **224** of an initial high electrical resistance state . . . [l]ower contact fuse element

224 operatively interconnects a lower counter electrode, such as a lower contact electrode **225** . . . ." This lower antifuse of dual damascene structure is not analogous to the capacitor element of the subject claim 1. In particular, as described by Lehmann *et al.* at paragraph [0004],

> "[A]n antifuse is an electrically programmable two-electrode device of small area on a semiconductor wafer, functioning as an electronic switch, and having a fuse element of fusible insulation, e.g., dielectric material, such as silicon dioxide, silicon nitride, or the like, of selective thickness, interposed between the two electrically conductive, e.g., metal or metallic, electrodes, i.e., an electrode and counter electrode. Upon activation by applying a programming voltage across the electrode and counter electrode to break down (cause a short in) the fusible insulation material and electrically interconnect the two electrodes, the antifuse irreversibly (permanently) changes from a high resistance, electrically non-conductive, unblown or 'off', state to a low resistance, electrically conductive, blown or 'on', state."

Therefore, the dielectric layer **224** of Lehmann *et al.* is a fuse element of an antifuse structure, and is broken down by applying a predetermined voltage to electrically connect an upper electrode to a lower electrode. Accordingly, the structure comprising electrode **225**, dielectric layer **224**, and antifuse **221** of Lehmann *et al.* is not a capacitor.

In turn, regarding claim 3, Lehmann *et al.* fails to disclose a method of manufacturing a semiconductor device comprising: forming capacitors having a bottom electrode, a dielectric layer and an upper electrode on a semiconductor substrate; forming a first insulating layer on the semiconductor substrate to cover the capacitors; the first insulating layer; forming a plurality of first via holes exposing surfaces of the bottom and upper electrodes by selectively patterning the first insulating layer; forming a plurality of first contact plugs by filling the first via holes with metal material; forming first metal wiring connected to the bottom electrodes through some of the first contact plugs and second contact plugs connected to the upper electrodes through the other first contact plugs, on the first insulating layer . . . as claimed in claim 3 of the subject application. As explained above, Lehmann *et al.* does not disclose a capacitor as specified in subject claim 1 and therefore does not teach or suggest a method of manufacturing such a semiconductor device comprising: forming capacitors having a bottom electrode, a dielectric layer and an upper electrode on a semiconductor substrate, as specified in claim 3.

It is a basic premise of patent law that, in order to anticipate, a single prior art reference must disclose within its four corners each and every element of the claimed invention. In *Lindemann v. American Hoist and Derrick Co.*, 221 USPQ 481 (Fed. Cir. 1984), the court stated:

> Anticipation requires the presence in a single prior art reference, disclosure of each and every element of the claimed invention, arranged as in the claim. *Connell v. Sears Roebuck and Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983); *SSIH Equip. S.A. v. USITC*, 718 F.2d 365, 216 USPQ 678 (Fed. Cir. 1983). In deciding the issue of anticipation, the [examiner] must identify the elements of the claims, determine their meaning in light of the specification and prosecution history, and identify corresponding elements disclosed in the allegedly anticipating reference. *SSIH, supra*; *Kalman [v. Kimberly-Clarke*, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)] (emphasis added). 221 USPQ at 485.

As Lehmann *et al.* does not teach the claimed capacitor, it does not teach each and every element of the subject invention. Therefore, it cannot anticipate. Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1 and 3 under 35 U.S.C. §102(e).

Claim 2 has been rejected under 35 U.S.C. §103(a) as obvious over Lehmann *et al.* in view of Knall *et al.* (U.S. 2002/0088998). Applicant respectfully traverses. A *prima facie* case of obviousness has not been presented. Three criteria must be met to establish *prima facie* case of obviousness. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the prior art reference, or combination of references, must teach or suggest all the claim limitations. See, *In re Dow Chemical Co.*, 5 USPQ2d 1529, 1531 (Fed. Cir. 1988).

The deficiencies of Lehmann *et al.* have been discussed above with respect to the rejection of claim 1, from which claim 2 depends. Knall *et al.* does not cure those defects. Knall *et al.* fails to provide any motivation to modify Lehmann *et al.* to include the capacitor element as claimed herein. Therefore, Applicant asserts that Lehmann *et al.* and Knall *et al.*, alone or in combination, cannot teach or suggest the subject invention of claim 2. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the §103(a) rejection of claim 2.

In view of the foregoing, Applicant believes that the currently pending claims are in condition for allowance, and such action is respectfully requested.

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 or 1.17 as required by this paper to Deposit Account 19-0065.

The applicant invites the Examiner to call the undersigned if clarification is needed on any of this response, or if the Examiner believes a telephonic interview would expedite the prosecution of the subject application to completion.

Respectfully submitted,

Jeff Lloyd
Patent Attorney
Registration No. 35,589
Phone No.: 352-375-8100
Fax No.: 352-372-5800
Address: Saliwanchik, Lloyd & Saliwanchik
A Professional Association
P.O. Box 142950
Gainesville, FL 32614-2950

JL/sjk/amh
Attachments: Request for Continued Examination including Petition and Fee for Extension of Time;
Replacement Drawings Sheets (Figures 4 and 5A-5D).

FIGURE 4

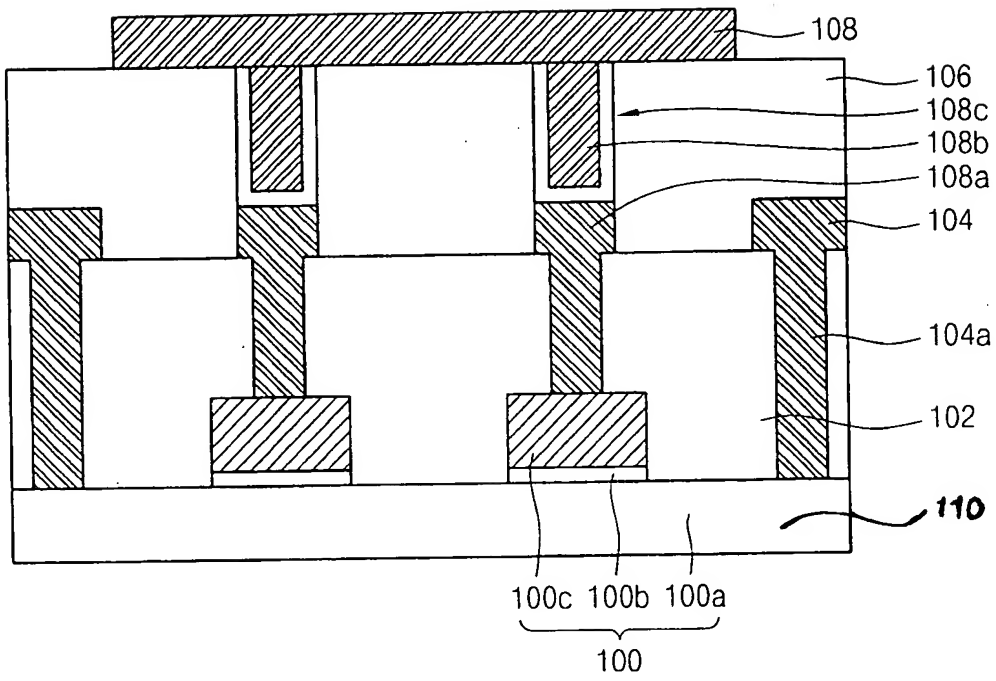

FIGURE 5A

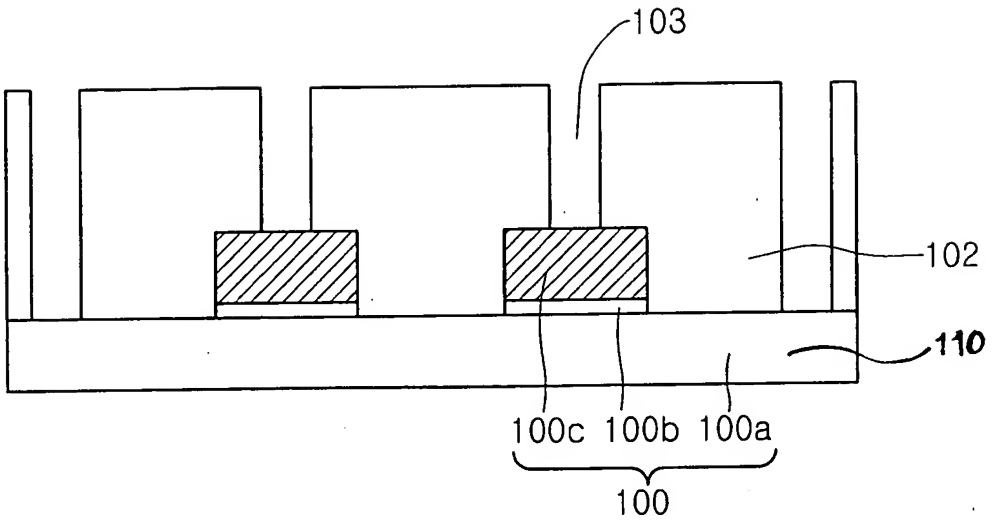

FIGURE 5B

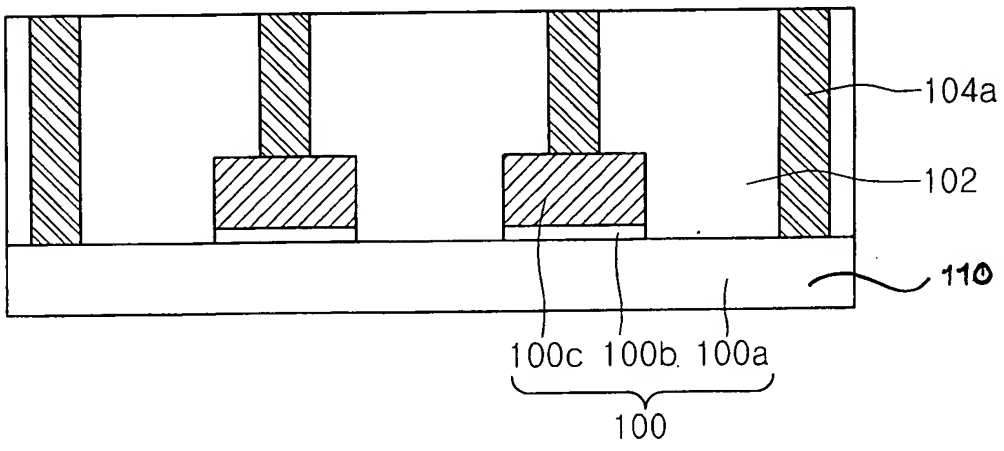

FIGURE 5C

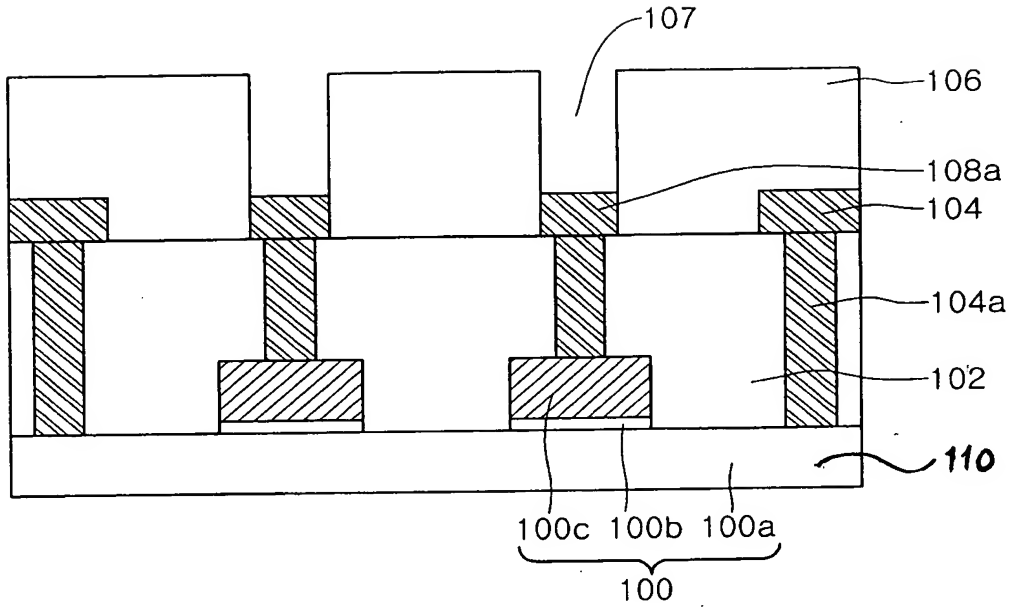

FIGURE 5D